ABSTRACT

In an RF power LDMOS transistor comprising multiple pairs of parallel gate fingers (11) located on opposite side of an associated p^+ sinker (23), and metal clamps (14) for short-circuiting the p^+ sinkers (23), each gate finger (11) of a pair is associated with separate metal clamps (14) that short-circuit the n^+ source region (20) and the p^+ sinker (23) associated with particular gate finger (11). The separate metal clamps (14) associated with each gate finger pairs are separated by a slot (15) that extends between the parallel gate fingers (11), and a metal runner (13) extends in the slot (15) between the separate metal clamps (14) associated with each finger pair from a gate pad. Both gate fingers (11) of a gate finger pair are connected to the associated metal runner (13) at both ends and at predetermined positions along their lengths.